ELECTRICAL & COMPUTER ENGINEERING

Lab 1: INTRODUCTION TO GATES AND DIGITAL LOGIC

The University of Washington | The Remote Hub Lab | Last Revised: March 2022

Summary

The goal of this lab is to build a foundational understanding of basic logic operators and logic gates. The lab introduces the AND, OR, NOR, XOR, and NAND operators, their corresponding gates, and the functions of a MUX.

Table of Contents

Why Should We Study Digital Logic?

Electronics are powered by electricity and the ability of electricity to be conceptualized into two states: an “off” or an “on” state. Usually, a zero (0) represents the off state (also known as the “false” state), and a one (1) represents the on state (also known as the “true” state).

How can only two representations -- a binary representation -- lead to complex technology? How can electronic devices (phones, computers, televisions, etc.) translate zeros and ones to information and applications? Under their cases, the devices contain fundamental circuits which rely on the basic components of digital logic. As a result, studying these building blocks is a key step in understanding how these devices work.

Before analyzing the zeros and ones of digital logic, it is important to understand the concept of inputs vs. outputs. A simple way to visualize this is to first view the inner workings of electronics as a “mystery box” system. We will understand the details later in this curriculum. For now, the key points are the following:

- First, some information enters the box as inputs.
- Then, some transformation happens inside the mystery box system.
- Finally, the changed information exits the system as output.

This input/output (I/O) relationship is shown in Figure 1.

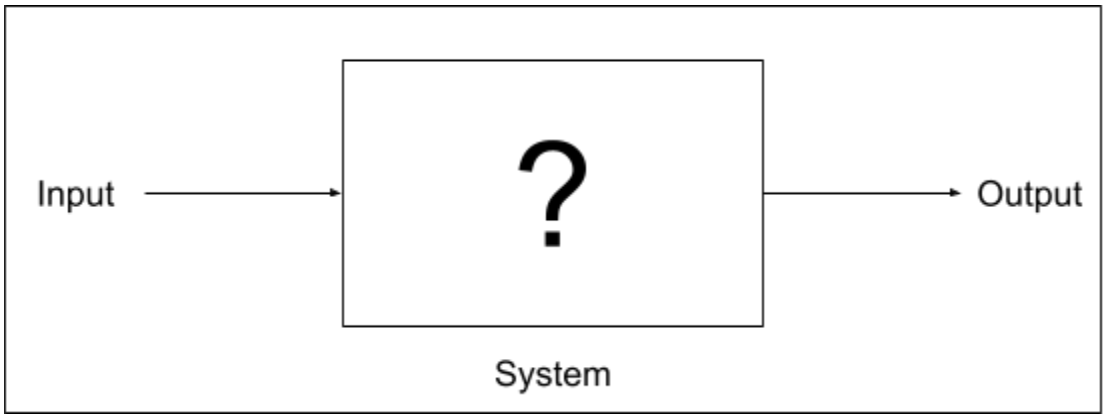

Figure 1: An Input/Output (I/O) System

Building on Figure 1 so the I/O components can be represented in binary format (zeros and ones), we can begin to analyze relationships between electronic components.

Logic Operators and Gates

Definitions of Basic Operators in Digital Logic

We will focus on five basic operators and one more special piece of hardware (MUX) defined as follows:

1. AND: For the output to be true, all inputs "AND-ed" together must be true.
2. OR: For the output to be true, at least one of the "OR-ed" inputs must be true.
3. NOR: For the output to be true, none of the "NOR-ed" inputs can be true.
4. XOR: For the output to be true, the number of true inputs "XOR-ed" together must be odd.
5. NAND: For the output to be true, the"NAND-ed" inputs cannot all be true.
6. MUX: A switch (control input) chooses between data inputs. Output is equal to the chosen input.

Logic Gates

Logic operators can be represented as logic gates. These gates are the hardware or physical components inside electronics. Figures 2-7 illustrate two-input representations of AND, OR, NOR, XOR, and NAND operators and a 3-input representation of the MUX. Accompanied with each figure are "equivalent notations" which preview Boolean Algebra expressions, a topic in "Lab 3: K-Maps and Boolean Algebra." (NOTE: The inverter or NOT gate (not shown) is implied by the bubble on NOR and NAND. It is equivalent to a "negation" denoted by the bar over a variable. The negation of 0 is 1; the negation of 1 is 0.)

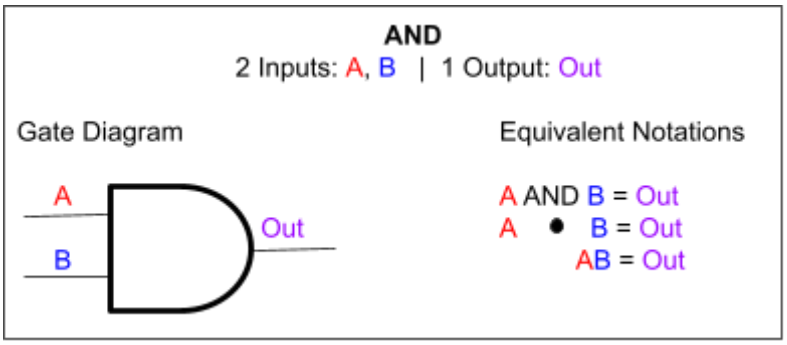

Figure 2: The "AND" Gate and Operator

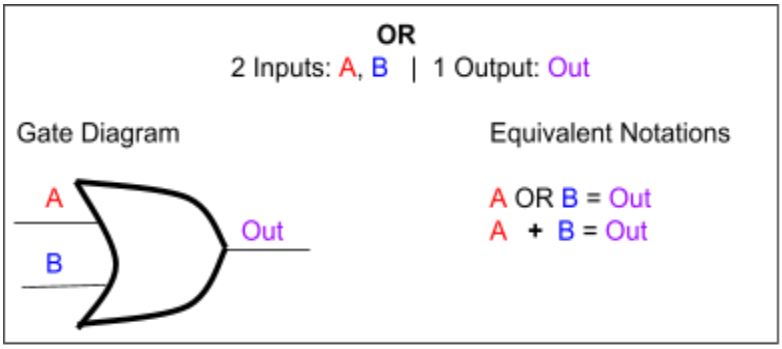

Figure 3: The "OR" Gate and Operator

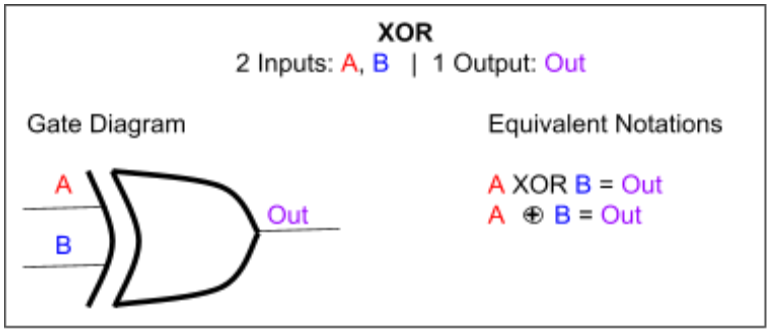

Figure 4: The "XOR" Gate and Operator

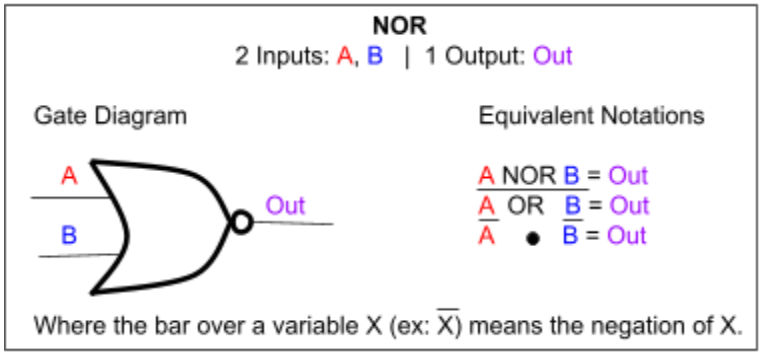

Figure 5: The "NOR" Gate and Operator

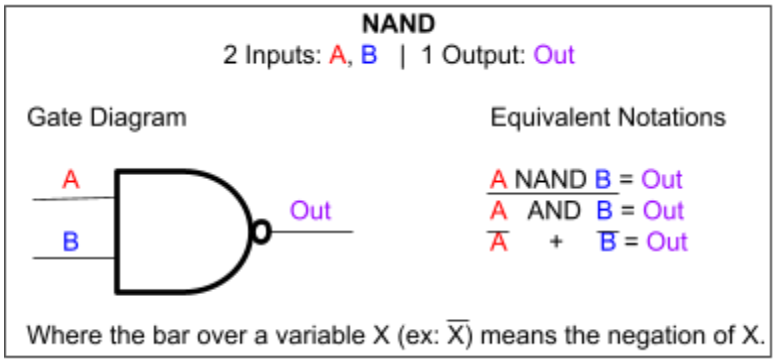

Figure 6: The "NAND" Gate and Operator

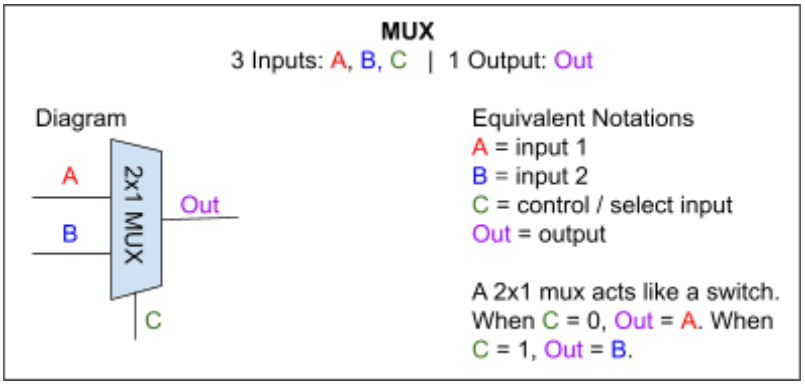

Figure 7: The Multiplexor "MUX"

LabsLand Activity

Premise

The Digital Trainer Activity builds intuition for the AND, OR, NOR, XOR, and NAND operators and the MUX -- the basic building blocks of digital logic. By experimenting with inputs and outputs (I/O) on remote hardware through LabsLand, you will learn how to distinguish relationships between these operators.

Digital Trainer Activity

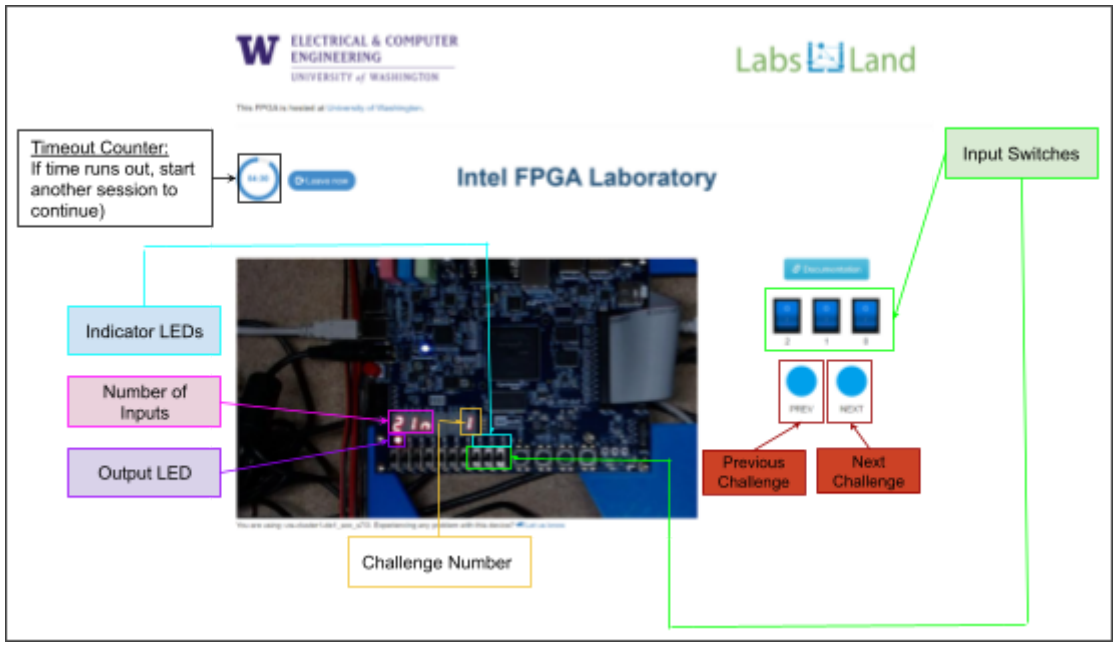

Figure 8: Digital Trainer Diagram

Instructions

1. Familiarize yourself with the LabsLand interface. (A diagram is shown in Figure 8.)
    a. The Field Programmable Gate Array (FPGA) board has 10 challenges pre-programmed.
    b. For each of the 10 challenges, notice that the HEX display (where the red digits and letters are on the FPGA) shows a label for the challenge number and the number of inputs in the challenge.
    c. Locate the blue input switches (Switch2, Switch1, and Switch0) on the right hand side of the screen.
    d. Locate the indicator LEDs (LED2, LED1, LED0) on the right hand side below the HEX display of the challenge number. These LEDs will be lit if their corresponding input switches (Switch2, Switch1, Switch0) are on; the LEDs will be off if their corresponding input switches are off.

e. Locate the output LED (LEDout) on the left hand side below the HEX display of the number of inputs. This LED will be on if an operator or mux applied to the system inputs results in a “true”; otherwise, the LED will be off.
f. Use the blue “Prev” and “Next” buttons to go to the previous or the next challenge respectively.

2. Using the definitions of basic operators, observe the output LEDs when the input switches are in different combinations of on and off. Note that a switch is “on” when it is flipped “up” and “off” when it is flipped “down.”

3. Based on your observations, record your initial thoughts in “Digital Trainer Observations” and your guess for the corresponding logic function on display for each challenge in “Digital Trainer Hypotheses and Logic Gates.”

Digital Trainer Observations

What do you notice about the output LED when the input switches are in different combinations of on and off? Which combinations result in the output LED being on vs. off? Notice that some challenges use 2 inputs, while others use 3 inputs (check the HEX display to find out the number of inputs in the challenge). Hints are given to help you start challenge 1.

- Challenge 1:
  - When Switch1 is false and Switch0 is false, LEDOut is _____.
  - When Switch1 is false and Switch0 is true, LEDOut is _____.
  - When Switch1 is true and Switch0 is false, LEDOut is _____.
  - When Switch1 is true and Switch0 is true, LEDOut is _____.

- Challenge 2:

- Challenge 3:

- Challenge 4:

- Challenge 5:

- Challenge 6:

- Challenge 7:

- Challenge 8:

- Challenge 9:

- Challenge 10:

Based on your observations, what operator do you suppose is on display for each challenge? Use Table 1 to record your guess for what logic function or operator is on display.

Table 1: Digital Trainer Hypotheses

Challenge	How many inputs?	What is the corresponding logic function or operator?				
1		AND	OR	NAND	NOR	XOR
2		AND	OR	NAND	NOR	XOR
3		AND	OR	NAND	NOR	XOR
4		AND	OR	NAND	NOR	XOR
5		AND	OR	NAND	NOR	XOR
6		AND	OR	NAND	NOR	MUX
7		AND	OR	NAND	NOR	MUX
8		AND	OR	NAND	NOR	MUX
9		AND	OR	NAND	NOR	MUX
10		AND	OR	NAND	NOR	MUX

Draw the corresponding logic gate or diagram of each of your guesses below.

Challenge 1:

Challenge 2:

Challenge 3:

Challenge 4:

Challenge 5:

Challenge 6:

Challenge 7:

Challenge 8:

Challenge 9:

Challenge 10:

Looking Ahead

Look back at Table 1 where you kept track of your hypotheses. Fill out Table 2 with your guess and a short description of why you chose that operator.

Table 2: Digital Trainer Reasoning

Challenge	Guess	Why did you choose this operator (1-2 sentences)?
1		
2		
3		
4		
5		

6		
7		
8		
9		
10		

These observations will help you in the following lab which introduces a graphic organizer called a “Truth Table”. The Truth Table is a mechanism for mapping I/O to zeros and ones which will help you determine if your guesses match the actual operator used in each of the 10 challenges.

Reflection and Observations

Lab 1 introduced you to logic gates and operators. Reflect on things you found interesting and/or challenging in the space below.

What questions do you still have, if any?